

ENHANCED CHIP SCALE PACKAGE FOR FLIP CHIPS

BACKGROUND OF THE INVENTION

The present invention generally relates to integrated circuits, and particularly
5 relates to chip scale packaging of flip chip integrated circuits.

Packaging technology represents an enabling element in the ongoing
microelectronics revolution. As integrated circuits have shrunk, so too have the physical
packages carrying these devices. Various techniques are used to minimize the physical
space required for integrated circuits, and to accommodate the increasingly high number
10 of signal connections associated with dense integrated circuit devices.

Common approaches include various chip-on-glass and chip-on-board
technologies. In these, an integrated circuit die is mounted directly on a primary circuit
substrate, covered only by a minimal amount of epoxy or resin. While offering certain
advantages in high-volume manufacturing environments, integrated circuit devices of
15 this nature place significant challenges on handling and testing.

Other approaches strike a balance between physical size and the practical
considerations of handling and testing. So-called "chip scale packages" (CSPs) attempt
to provide physical packaging for integrated circuit die without increasing the total
physical size substantially beyond that of the actual die. Ideally, such packages remain
20 as small as possible while still providing relatively robust protection for the die itself.

Chip scale packaging techniques may incorporate flip chip technology. With flip
chip technology, an integrated circuit die having connections on its top-side is literally
flipped over and mounted upside down to provide more direct interconnection to various
circuit elements within the die. In a CSP incorporating flip chip technology, an integrated
25 circuit die is flipped over and mounted top-side down to a chip carrier.

The chip carrier functions much like a printed circuit board, providing a rigid platform that can be readily handled and easily mounted to a larger circuit board carrying other electrical or electronic circuits. Essentially, the chip carrier provides practical access to the electrical interconnections of the flip chip it carries.

5 Typically, the chip carrier comprises a substrate having a top layer providing a number of conductive pads matched to the electrical connections of the flip chip. The flip chip is physically and electrically bonded to this top layer. Signal traces from the top layer pads are typically routed down through the substrate to its bottom layer. The bottom layer provides a set of conductive pads corresponding to the signal connections
10 of the flip chip mounted to the top-side of the substrate. Oftentimes, the bottom layer pads have an expanded spacing or "pitch" as compared to the top layer connections to facilitate design and manufacturing processes. Commonly, the bottom layer pads carry solder balls or the like, that allow the CSP to be soldered to a primary circuit board using any suitable technique, such as reflow soldering.

15 While CSPs incorporating flip chip technology provide opportunities for managing high I/O count devices while still maintaining a small overall size, they are not without potential disadvantages. For example, while the flip chip interconnection with the integrated circuit die helps minimize connection impedance, the overall connection impedance between signal points on the die and a primary circuit board on which the
20 CSP is mounted may still be excessive. The small size of the CSP may also be a disadvantage in terms of its thermal performance. The relatively high thermal impedance of conventional CSPs can be particularly problematic in high-performance devices.

BRIEF SUMMARY OF THE INVENTION

The present invention provides a chip scale package adapted to carry a flip chip integrated circuit die, and incorporates certain features enhancing the electrical and thermal performance of the package. A flip chip integrated circuit die mounts to a corresponding set of connection pads on the top layer of a chip carrier. The top layer pads are arranged such that the signal and ground interconnections between the chip carrier and a flip chip itself are interleaved. This interleaving creates a signal-ground-signal transmission line structure adapted to carry high-frequency signals with minimal loss and interference. The alternating signal and ground connections are routed down from the top layer to a bottom layer of the chip carrier where they are terminated in solder ball connections suitable for mounting the chip carrier to a primary circuit board. Preserving the signal and ground interleaving on all signal layers of the chip carrier minimizes cross-signal coupling and signal path impedances.

The bottom layer of the chip carrier further comprises a centralized ground plane that includes a number of so-called "thermal" vias terminating in the top layer of the chip carrier. These thermal vias provide interconnection paths between the top layer and the bottom layer ground plane with low electrical and thermal impedances. The low thermal impedance of the thermal vias allows heat energy to flow from the flip chip device into the bottom layer ground plane. The bottom layer ground plane further comprises a number of solder balls for physically and electrically connecting the ground plane to the primary circuit board. These solder balls directly connect the ground plane to the primary circuit and thus complete the low electrical and thermal impedance paths from the top side of the carrier.

BRIEF SUMMARY OF THE DRAWINGS

Fig. 1 is a diagram of a chip scale flip chip package assembly in accordance with present invention.

Fig. 2 is a simplified diagram of the alternating signal and ground transmission
5 line structure of the package assembly of Fig. 1.

Fig. 3 is a simplified diagram of selected thermal management features of the package assembly of Fig. 1.

Fig. 4 is a more detailed side view of the chip carrier used in the chip package of Fig. 1.

Fig. 5 is an exemplary top-side signal layer of the chip carrier.

Fig. 6 is an exemplary bottom-side signal layer corresponding to the top-side signal layer Fig. 5

Fig. 7 is a graph of measured transmission loss for an exemplary embodiment of the package assembly of Fig. 1.

Fig. 8 is a graph of measured reflection loss for the exemplary embodiment of Fig. 7.

Fig. 9 is a graph of modeled thermal performance for the exemplary embodiment of Fig. 7.

20 DETAILED DESCRIPTION OF THE INVENTION

Fig. 1 illustrates a chip scale package assembly in accordance with the present invention that is generally referred to by the numeral 8. The assembly 8 comprises a chip carrier 10, and a flip chip integrated circuit die 12. In use, the assembly 8 is customarily attached or mounted to another circuit, usually larger circuit board, referred
25 to herein as the primary circuit board 14.

The die 12 may be essentially any type of integrated circuit (IC), including digital, analog, or mixed-signal ICs. The die 12 includes a set of electrical connections on its top-side surface, which are generally implemented as a set of solder bumps 16. The solder bumps 16 provide contact points for making electrical interconnection between multiple signal and ground connections on the die 12 and the carrier 10. The die is referred to as a "flip chip" because it is flipped over, solder-bump side down for attachment to the chip carrier 10. In general, the set of solder bumps 16 form either a grid array or a perimeter array of contact points. For the purposes of this discussion, the solder bumps 16 are assumed to comprise a set of alternating signal and ground connections to the die 12 and are soldered to corresponding pads—discussed later—on the top side of the carrier 10. Often, an epoxy or resin under-fill 18 is used to seal the interface between the die 12 and the carrier 10.

The primary circuit 14 board is not part of the assembly 8, but is a common part of the environment in which the assembly 8 is used. Typically the primary circuit board 14 comprises a printed circuit board (PCB), sometimes referred to as a printed wiring board (PWB) that includes any number of integrated circuits, power supplies, connectors, and other types of electrical, or electro-mechanical devices. Generally, electrical interconnection between one or more of these other devices (not shown) and the die 12 is desired. Thus, the carrier 10 provides a mechanism for electrically and physically coupling the various signals of interest and ground connections on the die 12 with the primary circuit board 14. The carrier 10, as will be shown in more detail later, acts as a thermal conduit between the die 12 and the primary circuit board 14. The primary circuit board 14 itself acts as a heat sink to which the carrier 10 provides a low thermal impedance connection for the die 12.

The carrier 10 comprises a substrate 20, which may be a rigid, resin-based laminate, such as bismaleimide triazine (BT), or may be some other material with

appropriate characteristics as needed or desired. The substrate 20 has a top side 22 and a bottom side 24. The top side 22 includes a signal layer 26 and a solder mask layer 28, while the bottom side 24 includes a signal layer 30 and a solder mask layer 32. As will be shown later, the top-side signal layer 26 includes a number of connection points (pads) for interconnecting to the solder bumps 16 on the die 12, while the bottom-side signal layer 30 includes a number of connection points (pads) for electrically coupling the die 12 to the appropriate connections on the primary circuit board 14. The solder masks 28 and 32 generally cover the top and bottom signal layers 26 and 30, respectively, while leaving certain electrical connections on these layers exposed as needed.

The physical and electrical connections between the carrier 10 and the primary circuit board 12 are completed using solder balls 34 corresponding to signal and ground connections and thermal solder balls 36. The thermal solder balls 36 provide low thermal impedance coupling between a bottom-side planar heat sink 38 of the carrier 10 and the primary circuit board 14.

The carrier 10 also includes characteristics contributing to electrical signal integrity between the die 12 and associated circuitry on the primary circuit board 14. This good signal integrity allows the flip chip die 12 to operate at signal frequencies up to and in excess of 6 GHz with 0.5 dB of insertion loss. Of course, thermal management becomes a significant concern for the die 12, particularly at GHz operating frequencies. The following discussion and accompanying diagrams highlight several features of the carrier 10 that contribute to its excellent electrical and thermal performance.

Fig. 2 is a simplified schematic representation of the carrier 10, and illustrates the electrical coupling it provides between the die 12 and the primary circuit board 14. The top side 22 of the carrier 10 includes a set of top-side pads 40. This set of top-side pads 40 provide electrical connections for the corresponding set of solder bumps 16 on the

die 12. In this exemplary embodiment, the top-side pads 40 are disposed in the top-side signal layer 26, and arranged in an perimeter array of alternating signal and ground connections, in accordance with the signal and ground connections on the die 12. The bottom side 24 of the carrier 10 includes a set of bottom-side pads 42, arranged here as
 5 an outer array of bottom-side pads 42A and an inner array of bottom-side pads 42B.

Respective ones of the top-side pads 40 connect with respective ones of the bottom-side pads 42 through corresponding conductive paths 44. The solder balls 34 shown in Fig. 1 are individually attached to the bottom-side pads 42 for coupling to corresponding electrical connections on the primary circuit board 14. Thus, a top-side
 10 pad 40, along with corresponding conductive path 44, bottom-side pad 42, and solder ball 34, form an electrical connection between the die 12 and the primary circuit board 14. Each conductive path 44 typically includes a top-side conductive trace 46 disposed in the top-side signal layer 26 coupling its corresponding top-side pad 40 to a via 48, which provides an electrically conductive path through the substrate 20. A bottom-side
 15 conductive trace 50 typically disposed in the bottom-side signal layer 30 couples the via 48 to a corresponding one of the bottom-side pads 42.

In the exemplary arrangement, the outer and inner arrays of bottom-side pads 42A and 42B, respectively, form parallel rows of staggered pads 42 in an alternating signal and ground arrangement along each side of the carrier 10. The conductive paths
 20 44 and their corresponding bottom side pads 42 preserve the alternating signal and ground connection arrangement established between the die's solder bumps 16 and the top-side pads 40. This arrangement interposes a ground-carrying conductive path 44 between signal-carrying paths 44. This alternating signal and ground connection arrangement between the die 12 and the primary circuit board 14 provided by the carrier
 25 10 may be observed by noting the "S" and "G" designations in the illustration, corresponding to signal and ground connections, respectively.

In effect, the alternating signal and ground top-side and bottom-side pads 40 and 42, respectively, and the corresponding interconnecting conductive paths 44, provide a transmission line structure for electrical connections between the die 12 and the circuit board 14, which minimizes signal cross talk. Cross talk minimization contributes to the ability of the chip scale package assembly 8 of the present invention supporting operation of the flip chip die 12 at frequencies in excess of 6 GHz with 0.5 dB of insertion loss. Note that for the sake of simplicity, the diagram illustrates a limited number of top-side pads 40 and bottom-side pads 42. The extent to which alternating signal and ground connections may be established depends on the total number of pads 40 and 42, and the connection pattern illustrated is exemplary only.

Other features contribute to the ability of the chip scale package assembly 8 to support operation at such high frequencies. Fig. 3 illustrates several of these additional features relating both to signal integrity and thermal management. The top side 22 of the carrier 10 includes a mounting area 52 for receiving the die 12. The perimeter of the mounting area 52 is generally defined by the array of top-side pads 40 (see Fig. 2). One or more thermal vias 54 are disposed within the mounting area 52 and connect with the bottom-side planar heat sink 38. In this exemplary embodiment, the bottom-side comprises a ground plane 38, which is typically implemented as a copper plane on the bottom side 24 of the carrier 10 that is connected to electrical ground, and which enhances thermal performance of the carrier 10.

Each thermal via 54 extends vertically down into the ground plane 38 on the bottom side 24 of the carrier 10. The thermal vias 54 act as low thermal impedance heat conduits, efficiently conducting heat generated by the die 12 down into the ground plane 38, which acts as a heat sink for the die 12. Because each thermal via 54 is electrically and thermally bonded to the ground plane 38, the thermal vias 54 also provide low electrical impedance ground paths for the flip chip die 12.

The ground plane 38 couples to the primary circuit board 14 using a number of so-called thermal solder balls 36 that are directly coupled to the ground plane 38. In manufacturing, the chip carrier 10 is soldered to the primary circuit board 14 using the thermal solder balls 36, as well as the signal- and ground-carrying solder balls 34 that are attached to the bottom-side pads 42A and 42B. By directly coupling the ground plane 38 to the primary circuit board 14 through the thermal solder balls 36, low electrical and thermal impedance paths are established between the die 12 and the primary circuit board 14. The primary circuit board 14 may include its own heat sinking features (not shown) such as copper planes to which the thermal solder balls 36 may be bonded.

Fig. 4 shows a simplified side view of the package assembly 8 that illustrates the signal and ground vias 48, as well as the thermal vias 54. Top-side pads 40 interconnect with corresponding ones in a set of signal- and ground-carrying vias 48 that form portions of the conductive paths 44 discussed earlier. These vias 48 are coupled to corresponding ones of inner and outer bottom-side pads 42A and 42B, respectively. The signal and ground connections from the bottom-side pads 42 are made with the primary circuit board using solder balls 34, with one solder ball 34 attached to each of the bottom-side pads 42. The thermal vias 54 positioned beneath the die 12 provide, as earlier noted, thermally conductive paths from the die 12 into the ground plane 38.

Fig. 5 provides a more detailed view of the top-side signal layer 26 in an exemplary implementation of the carrier 10. The top-side pads 40 are electrically coupled to corresponding ones of the signal- and ground-carrying vias 48 by the top-side traces 46, which form portions of the conductive paths 44. Fig. 5 also shows the thermal vias 54 centrally positioned inside the inner ring of vias 48.

Fig. 6 illustrates the bottom-side signal layer 30 corresponding to the top-side layer 26 of Fig. 5, and depicts the outer and inner rectangular perimeters formed by the

bottom-side pads 42A and 42B, respectively. Respective ones of the conductive traces 50 form portions of the conductive paths 44 and couple the bottom-side pads 42 to corresponding ones of the vias 48. Note that a portion of the vias 48 are arrayed about the perimeter formed by the outer array of bottom-side pads 42A, while a remaining

5 portion of the vias 48 are arrayed about the inside of the perimeter formed by the inner array of bottom-side pads 42B. Also note that the alternating signal-ground-signal pattern is preserved between the top-side signal layer 26 and the bottom-side signal layer 30.

Fig. 6 further depicts the bottom-side ground plane 38, and shows the

10 arrangement of the thermal vias 54 and thermal solder balls 36 relative to the ground plane 38. Note that a number of the ground-carrying bottom-side conductive traces 50 are connected to the ground plane 38. These connections further reduce the electrical impedance of the ground connections established between the die 12 and the primary circuit board 14.

15 Fig. 7 illustrates measured insertion loss of the carrier 10. The diagram clearly shows that about 6 GHz and 17 GHz, the insertion loss is -0.5 dB and -3 dB, respectively. This performance enables use of the carrier 10 in high frequency flip chip applications ranging at least to 6 GHz, and also enables use in high-speed digital applications, such as those having clock speeds of about 2 to 3 GHz. The graph

20 assumes a 5 mm x 5 mm size for the carrier 10 using the top-side signal layer 26 and the bottom-side signal layer 30 arrangements shown in Figs. 5 and 6, respectively. The horizontal axis plots frequency from 50 MHz to 18 GHz, while the vertical axis depicts transmission loss magnitude in dB. As shown, transmission loss through the carrier 10 between the die 12 in the primary circuit board 14 exhibits excellent transmission

25 performance, with only 0.5 dB of insertion loss up to 6 GHz.

Fig. 8 depicts reflection loss for the package assembly 8 based on the same implementation details on which Fig. 7 is based. Again, the horizontal axis depicts frequency from 50 MHz to 18 GHz, while the vertical axis depicts reflection loss magnitude in dB.

5 While Figs. 7 and 8 depict measured electrical performance of the package assembly 8, Fig. 9 illustrates modeled thermal performance of the chip scale package 8 of the present invention implemented in accordance with the details of Figs. 5 and 6 compared with a similar package assembly that omits the ground plane 38, the thermal solder balls 36, and the thermal vias 54. The vertical axis depicts modeled junction to air
10 thermal resistance for the die 12 in degrees centigrade per watt ($^{\circ}\text{C}/\text{W}$). The thermal simulation model has been validated with measurements. Maximum power dissipation is predicted as 1.54 Watts using industry-standard measurement conditions and thermal window. As shown, the low impedance thermal paths established between the die 12 and the primary circuit board 14 in the package assembly 8 of the present invention
15 provide substantial reduction in thermal resistance.

In exemplary embodiments, the present invention provides a chip scale package assembly 8 adapted to mount a flip chip die 12 to a primary circuit board 14, and to provide low electrical and thermal impedance connections between the die 12 and the board 14. The present invention is subject to variation in its implementation details and
20 as such, the above discussion and accompanying drawings provide details for exemplary embodiments only, and should not be construed as limiting the invention. Indeed, the present invention is limited only by the following claims and the reasonable equivalents thereof.